IMPLEMENTATION PLAN

**Instructions**

Table

Description automatically generated

R-type: add, subtract, and, or

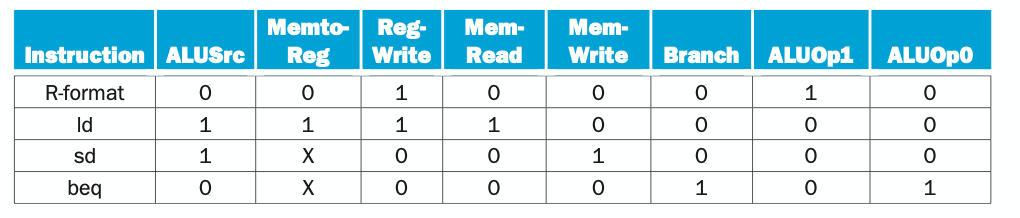
memory: ld, sd

branch: beq

\* Task 1: Read each instruction (add x1,x2,x5) and convert to 32 bit address.

\* Task 2: From first 7 bits, derive control variables.

\* Task 3: Construct Simulator Class.



Table

Description automatically generated

Diagram, schematic

Description automatically generated

Diagram

Description automatically generated